

Notice of References Cited	Application/Control No. 10/023,723		Applicant(s)/Patent Under Reexamination CHANDRAN ET AL.	
	Examiner James M. Mitchell		Art Unit 2813	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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*	B	US-6,330,967	12-2001	Milewski et al.	228/180.22
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NON-PATENT DOCUMENTS

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	V	Xiao, "The Effect of Cu Stud structure and Eutectic Solder Electroplating on Intermetallic Growth and Reliability of Flip-Chip Solder Bump", 09/2000, IEEE, Pg. 54-59
	W	Wang, "Studies on A Novel Flip-Chip Interconnect Structure-Pillar Bump", 04/2001, IEEE
	X	Karim, "Lead-Free Bump Interconnections for Flip-Chip Applications", 01/2000, IEEE, pg 274-278

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.